

silicon layer.

56. (New) The intermediate of claim 40 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

57. (New) The intermediate of claim 56 wherein the first and second polycrystalline silicon layers are doped with arsenic.

58. (New) The intermediate of claim 41 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

Bl
Cmt
59. (New) The intermediate of claim 58 wherein the first and second polycrystalline silicon layers are doped with arsenic.

60. (New) The intermediate of claim 42 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

61. (New) The intermediate of claim 43 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

62. (New) The intermediate of claim 44 wherein a photoresist mask is applied over a portion of the first etch stop layer and the second polycrystalline silicon layer.

63. (New) The intermediate of claim 62 wherein a titanium layer is deposited to overlie the etch stop layer and the second polycrystalline silicon layer.

64. (New) The intermediate of claim 45 wherein the polycrystalline plug and the polycrystalline silicon layer are doped to increase their conductivity.

65. (New) The intermediate of claim 64 wherein the polycrystalline plug and the polycrystalline silicon layer are doped with arsenic.

66. (New) The intermediate of claim 46 wherein the polycrystalline plug is doped to increase its conductivity.

67. (New) The intermediate of claim 66 wherein the polycrystalline plug is doped with arsenic.

68. (New) The intermediate of claim 47 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

69. (New) The intermediate of claim 68 wherein the first and second polycrystalline silicon layers are doped with arsenic.

*Bl
Cmt*

70. (New) The intermediate of claim 48 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

71. (New) The intermediate of claim 70 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

72. (New) The intermediate of claim 49 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

73. (New) The intermediate of claim 72 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

74. (New) The intermediate of claim 50 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

75. (New) The intermediate of claim 74 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

76. (New) The intermediate of claim 51 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

77. (New) The intermediate of claim 76 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

*BJ
Cancelled*
78. (New) The intermediate of claim 52 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

79. (New) The intermediate of claim 78 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

Serial Number: 09/745,780

Filing Date: December 21, 2000

Title: METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS

Claims 38-79 are now pending in this application. Newly added claims 53-79 are each dependent upon one of claims 38-52. The Examiner is invited to contact Applicant's Representatives at the below-listed telephone number if there are any questions regarding this Response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

MARTIN CEREDIG ROBERTS ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6970

Date August 23, 2001

By


Charles E. Steffey
Reg. No. 25,179

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 23 day of August, 2001.

Name

Tina Pugh

Signature

